AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS

1. (currently amended) A controller chip comprising:

a graphics engine operative to manage a memory, the graphics engine comprising an integral interface; and

a circular first in first out (FIFO) buffer coupled to the graphics engine, the circular FIFO buffer being accessible by a central processing unit (CPU) through the graphics engine, wherein the graphics engine receives commands from the CPU via the integral interface, and manages the circular FIFO buffer via the integral interface and wherein all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the FIFO buffer as viewed by the CPU can be as large as the memory.

2. (canceled)

3. (canceled)

4. (currently amended) The controller chip of claim 1 in which the circular FIFO buffer comprises a double buffer.

5. (currently amended) The controller chip of claim 1 in which the circular FIFO buffer comprises a triple buffer.

6. (canceled)

7. (currently amended) The controller chip of claim 1 which includes a checking mechanism for determining if the circular FIFO buffer needs to be emptied without utilizing the CPU.

8. (currently amended) The controller chip of claim 7 wherein the checking mechanism comprises:

means for calculating the time required to fill the circular FIFO buffer;

means for determining if the used memory of the circular FIFO buffer, is below a predetermined amount based upon the time required to fill the circular FIFO buffer; and

means for preventing the circular FIFO buffer from filling if the used memory in the circular FIFO buffer is over the predetermined amount.

9. (original) The controller chip of claim 1 wherein the controller chip comprises a graphics controller chip.

10. (original) The controller chip of claim 9 wherein the engine comprises a graphics engine.

11. (currently amended) A system for providing a command stream in a computer system comprising:

a central processing unit (CPU);

a controller coupled to the CPU and including a graphics engine comprising an integral interface;

a memory coupled to the controller, the memory being managed by the controller; and

a circular first in first out (FIFO) buffer coupled to the controller, the circular first in first out (FIFO) buffer being accessible by the CPU through the controller, wherein the controller

receives commands from the CPU via the integral interface, manages the storage element via the integral interface and writes the commands into the memory and wherein all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the FIFO buffer as viewed by the CPU can be as large as the memory.

12. (canceled)

13. (canceled)

14. (currently amended) The system of claim 11 in which the circular FIFO buffer comprises a double buffer.

15. (currently amended) The system of claim 11 in which the circular FIFO buffer comprises a triple buffer.

16. (previously presented) The system of claim 11 in which the controller comprises a graphics controller.

17. (canceled)

18. (currently amended) The system of claim 11 which includes a checking mechanism for determining if the circular FIFO buffer needs to be emptied without utilizing the CPU.

19. (currently amended) The system of claim 18 wherein the checking mechanism comprises:

means for calculating the time required to fill the circular FIFO buffer;

means for determining if the circular FIFO buffer is below a predetermined amount based upon the time required to fill the buffer; and

means for preventing the circular FIFO buffer from filling if the circular FIFO buffer is above the predetermined amount.

20. (currently amended) A method for providing a command stream in a computer system, the computer system including a central processing unit (CPU), a controller coupled to the CPU, a memory coupled to the controller, the memory being managed by the controller, the method comprising the steps of:

(a) providing a circular first in first out (FIFO) buffer within the controller; and

(b) allowing the circular FIFO buffer to be accessible by the CPU via an integral interface of a graphics engine of the graphics controller wherein all data transmittable to the circular FIFO buffer is transmitted via the integral interface and the effective size of the FIFO buffer as viewed by the CPU can be as large as the memory.

21. (canceled)

22. (canceled)

23. (currently amended) The method of claim 20 in which the circular FIFO buffer comprises a double buffer.

24. (currently amended) The method of claim 20 in which the circular FIFO buffer comprises a triple buffer.

25. (previously presented) The method of claim 20 in which the memory comprises a graphics memory.

26. (canceled)

27. (currently amended) The method of claim 20 which includes the step of (c) determining if the circular FIFO buffer needs to be emptied without utilizing the CPU.

28. (currently amended) The method of claim 27 wherein the determining step (c) further comprises:

(c1) calculating the time required to fill the circular FIFO buffer;

(c2) determining if the circular FIFO buffer is below a predetermined amount based upon the time required to fill the buffer; and

(c3) preventing the circular FIFO buffer from filling if the circular FIFO buffer is above the predetermined amount.